

**WHAT IS CLAIMED IS:**

1. A method for forming a multilayer interconnect, comprising:
  - a first step of forming a lower layer interconnect in an upper portion of a first insulating film and then forming a second insulating film and a third insulating film in this order on the first insulating film including the lower layer interconnect;
  - a second step of forming an aperture in part of the third insulating film located above the lower layer interconnect;
  - a third step of forming an interconnect groove in an upper portion of the third insulating film so that an upper portion of the aperture is part of the interconnect groove,
  - 10 while reducing the thickness of part of the second insulating film located under the aperture without having the lower layer interconnect exposed;
  - a fourth step of removing part of the second insulating film located under the aperture to expose the lower layer interconnect; and
  - a fifth step of filling a conductive film in the aperture and the interconnect groove
  - 15 and thereby forming an upper layer interconnect and a connection portion for electrically connecting the upper layer interconnect and the lower layer interconnect.

2. The method of claim 1, wherein the second step includes reducing the thickness of part of the second insulating film located under the aperture.

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3. The method of claim 2, wherein the second and third insulating films are formed of silicon nitride and silicon oxide, respectively,
  - wherein in the second step, the aperture is formed by dry etching using a first etching gas containing a fluorocarbon gas and an oxygen gas, and
  - 25 wherein in the third step, the interconnect groove is formed by dry etching using a

second etching gas containing a fluorocarbon gas and an oxygen gas.

4. The method of claim 3, wherein in the second step, the ratio of the fluorocarbon gas to the oxygen gas in the first etching gas and the ratio of carbon to fluoride in the 5 fluorocarbon gas are adjusted to control the depth of part of the second insulating film located under the aperture.

5. The method of claim 3, wherein in the third step, the ratio of the fluorocarbon gas to the oxygen gas in the second etching gas and the ratio of carbon to fluoride in the 10 fluorocarbon gas are adjusted to control the depth of part of the second insulating film located under the aperture.

6. The method of claim 1, further comprising the step of forming a reflection-prevention film over the second insulating film,  
15 wherein the second step includes removing part of the reflection-prevention film in which the aperture is to be formed, and  
wherein the third step includes removing part of the reflection-prevention film in which the interconnect groove is to be formed.

20 7. The method of claim 6, wherein the reflection-prevention film is formed of silicon oxide nitride so as to have a smaller thickness than that of the second insulating film, and  
wherein in the third step, the reflection-prevention film is removed by etching under the condition where the temperature of a lower electrode of an etching apparatus is  
25 30 C° or more.

8. The method of claim 1, wherein in the fourth step, the lower layer interconnect is exposed by etching under the condition where bias power for an etching apparatus is 500 W or less.

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9. A method for checking a multilayer interconnect, the multilayer interconnect being formed in a formation method including: a first step of forming a lower layer interconnect in an upper portion of a first insulating film and then forming a second insulating film and a third insulating film in this order on the first insulating film including 10 the lower layer interconnect; a second step of forming an aperture in part of the third insulating film located above the lower layer interconnect; a third step of forming an interconnect groove in an upper portion of the third insulating film so that an upper portion of the aperture is part of the interconnect groove, while reducing the thickness of part of the second insulating film located under the aperture without having the lower layer 15 interconnect exposed; a fourth step of removing part of the second insulating film located under the aperture to expose the lower layer interconnect; and a fifth step of filling a conductive film in the aperture and the interconnect groove and thereby forming an upper layer interconnect and a connection portion for electrically connecting the upper layer interconnect and the lower layer interconnect, comprising the steps of:

20 forming a checking lower layer interconnect in the upper portion of the first insulating film and then forming the second insulating film and the third insulating film in this order over the first insulating film including the checking lower layer interconnect;

forming a checking aperture in part of the third insulating film located above the checking lower layer interconnect in the same manner as in the second step;

25 forming an interconnect groove in an upper portion of the third insulating film in

the same manner as in the third step so that an upper portion of the aperture is part of the interconnect groove;

filling a conductive film in the checking aperture and the checking interconnect groove and thereby forming a checking electrode and a checking upper layer interconnect,  
5 respectively;

applying a predetermined voltage to the checking lower layer interconnect and the checking upper layer interconnect to check whether or not the checking lower layer interconnect and the checking upper layer interconnect are electrically continuous; and

determining that the lower layer interconnect is not to be exposed by the third step  
10 if the checking lower layer interconnect and the checking upper layer interconnect are not electrically continuous, and that the lower layer interconnect is to be exposed by the third step if the checking lower layer interconnect and the checking upper layer interconnect are electrically continuous.

15 10. The method of claim 9, wherein the checking electrode is arranged in parallel to the checking lower layer interconnect and the checking upper layer interconnect.